PLEASE NOTE THAT THIS APPLICATION IS
ASSOCIATED WITH A CUSTOMER NUMBER. PLEASE
INPUT THE CUSTOMER NUMBER LOCATED BENEATH
THE SIGNATURE LINE OF THE ATTORNEY.

THANK YOU

TITLE

DEEP TRENCH SELF-ALIGNMENT PROCESS FOR AN ACTIVE AREA OF A PARTIAL VERTICAL CELL

BACKGROUND OF THE INVENTION

5   **Field of the Invention**

The invention relates to a deep trench self-alignment process, and more particularly to a deep trench self-alignment process for an active area of a partial vertical cell and a method for fabricating the same.

10   **Description of the Related Art**

There is much interest in reducing the size of individual semiconductor devices to increase their density on an integrated circuit (IC) chip. This reduces size and power consumption of the chip, and allows faster operation of the

15   chip. In order to achieve a memory cell with a minimum size, the gate length in a conventional transistor must be reduced to decrease the lateral dimension of the memory cell. However, the shorter gate length results in higher leakage current that cannot be tolerated, and the voltage on the bit line must

20   therefore also be scaled down. This reduces the charges stored on a storage capacitor, thus requiring a larger capacitance to ensure that stored charges are accurately detected.

In order to solve the above-mentioned problems, a stacked capacitor and a deep trench capacitor have been developed for

25   a high-integration memory cell, such as dynamic random access memory (DRAM) cell. Specifically, the deep trench capacitor is formed in a deep trench within the silicon substrate, such that the capacitor storage region does not take up any additional

1

wafer area. In addition, a vertical transistor has recently been developed which can maintain gate length of a suitable value to reduce leakage without decreasing the bit line voltage or increasing the memory cell's lateral dimensions.

5   A type of vertical transistor with a deep trench capacitor is disclosed in U.S. No. 6,034,389.

FIGs. 1a to 1e are cross-sections of the conventional method for fabricating a floating gate of a split gate flash memory.

10   In FIG. 1a, a P-type silicon substrate 101 comprises a plurality of deep trenches 104 and a plurality of pillars 102 corresponding to the deep trenches 104.

A thin pad oxide layer 103a and an oxynitride layer 103b are sequentially formed on the surface of the pillar 102. A

15   doped oxide layer 105, such as ASG, acting as a source region diffusion source is formed on a bottom sidewall of the deep trench 104. The doped oxide layer 105 is annealed at a high temperature and a short time to diffuse As ions into the sidewall of the pillar 102 to form an n+ type diffusion region acting

20   as an n+ type source region 106.

In FIG. 1b, the doped oxide layer 105 is removed.

In FIG. 1c, an ONO thin film 107 is formed on the sidewall of the deep trench 104 acting as a dielectric material of the deep trench capacitor. An n+ type poly layer 108 is formed

25   in the deep trench 104 acting as a capacitor plate. The ONO thin film 107 and the capacitor plate 108 are etched to a predetermined depth.

In FIG. 1d, a shelter 109 is formed on the n+ poly layer 108 acting as a gate insulator. A gate oxide layer 110 is formed

30   on the sidewall of the deep trench 104, and the deep trench

104 is filled with an n+ poly layer 111 acting as a control gate.

In FIG. 1e, the control gate 111 is separated into word lines by etching. The thin pad oxide layer 103a and oxynitride layer 103b are removed. An n+ drain 112 is formed in the top of the pillar 102. A metal layer is formed acting as a bit line layer 113. Thus, a memory unit array is completed.

According the above-described memory cell, the n^+-type polysilicon layers 111, the n^+-type source region 106 and the n^+-type drain region 112 form the vertical transistor, and the n^+-type source region 106, the ONO thin film 107 and the n^+-type polysilicon layers 108 form the deep trench capacitor. In an open bit line case as described, the storage node of the deep trench capacitor is common to all the memory cells in the array, and the charge is stored on the n^+-type source region 106 within each pillar 102.

Although a channel occurs in the pillar 102 between n+ source region 106 and n+ drain region 112, the width of the pillar 102 cannot be reduced to avoid the depletion regions overlapping adjoining source regions 106 on the sidewall of the pillar 102.

The dopant in the capacitor easily diffuses to the active area when the active area in the pillar 102 is misaligned with the deep trench 104. The electrical properties of the memory cell are affected by the dopant concentration of the active area.

SUMMARY OF THE INVENTION

The present invention is directed to a deep trench self-alignment process for an active area of a partial vertical cell by filling an ARC layer in the deep trench.

5 Accordingly, the present invention provides a deep trench self-alignment process for an active area of a partial vertical cell. A semiconductor substrate with two deep trenches is provided. A deep trench capacitor is formed in each deep trench, and an isolating layer is formed thereon. Each trench 10 is filled with a mask layer. A photoresist layer is formed on the semiconductor substrate between the deep trenches, and the photoresist layer partially covers the mask layer surface. The semiconductor substrate is etched lower than the isolating layer using the photoresist layer and the mask layer as masks. 15 The photoresist layer and the mask layer are removed, such that the pillar semiconductor substrate between the deep trenches functions as an active area.

Accordingly, the present invention provides another deep trench self-alignment process for an active area of a partial 20 vertical cell. A semiconductor substrate with a pad layer is provided. Two deep trenches are formed in the semiconductor substrate separated by a predetermined distance. A deep trench capacitor is formed in each deep trench, below the semiconductor substrate, and a ring-shaped insulating layer is formed on 25 a top sidewall of each deep trench. An isolating layer is conformally formed on the semiconductor substrate and the deep trenches. The isolating layer on the sidewall of the deep trench is removed to leave the isolating layer on the surface of the deep trench capacitor. A mask layer is formed on the

4

semiconductor substrate, and the deep trench is filled with the mask layer. The mask layer is planarized until the semiconductor substrate is exposed to leave the mask layer in the deep trenches. A photoresist layer is formed on the

5   semiconductor substrate between the deep trenches. The photoresist layer partially covers the hard mask layer surface. The semiconductor substrate is etched to below the isolating layer by a predetermined depth using the photoresist layer and the mask layer as etching masks. The photoresist layer

10   and the mask layer are removed, such that the pillared semiconductor substrate acts as an active area between the deep trenches.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention,

15   reference is made to a detailed description to be read in conjunction with the accompanying drawings, in which:

FIGs. 1a to 1e are cross-sections of the conventional method for fabricating a floating gate of a split gate flash memory;

20   FIGs. 2a to 2h are cross-sections of the deep trench self-alignment process for an active area of a partial vertical cell of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGs. 2a to 2h are cross-sections of the deep trench

25   self-alignment process for an active area of a partial vertical cell of the present invention.

In FIG. 2a, a semiconductor substrate 201, such as silicon, with a pad layer 202, such as a pad oxide layer or a pad nitride

layer, is provided. Two deep trenches 201a are formed in the semiconductor substrate 201 separated by a predetermined distance acting as an active area defined in subsequent process. The predetermined distance is about 1200 to 1400Å.

5   Each deep trench 201a is filled with a conducting layer, such as poly layer, acting as a deep trench capacitor 203. The deep trench capacitor 203 is lower than the top surface of the semiconductor substrate 201 by a predetermined depth. A channel length of a subscript vertical MOS is defined by

10   the predetermined depth. A ring-shaped insulating layer 204, such as collar oxide layer, is formed on a top sidewall of each deep trench 201a as gate isolation.

In FIG. 2b, an isolating layer is conformally formed on the semiconductor substrate 201, the deep trenches 201a, and

15   deep trench capacitors 203. The isolating layer is anisotropically etched to remove the isolating layer from the sidewall of the deep trenches 201a, and an isolating layer 205, such as top trench oxide (TTO) layer, remains on the deep trench capacitors 203. The ratio of the isolating layer on

20   the deep trench 201a sidewall to the isolating layer on the capacitor 203 surface is less than 1:8. The thickness of the isolating layer on the capacitor 203 surface is not significantly affected by etching of the isolating layer from the deep trench sidewall.

25   In FIG. 2c, a mask layer 206, such as organic anti-reflection coating layer, is formed on the pad layer 202, and the deep trenches 201a are filled with the mask layer 206. The organic anti-reflection coating layer is a SiON layer.

In FIG. 2d, the mask layer 206 is planarized by CMP or etching to expose the pad layer 202 and leave the mask layer 206a in each deep trench 201a.

In FIG. 2e, a photoresist layer 207 is formed on the semiconductor substrate 201 between the deep trenches 201a, partially covering the mask layer 206a.

In FIG. 2f, the semiconductor substrate 201 is anisotropically etched by plasma etching or reactive ion etching using the photoresist layer 207 and the mask layer 206a as etching masks until the non-covered semiconductor substrate 201 is lower than the isolating layer 205 by a predetermined depth of about 2600 to 3300Å. The plasma etching or reactive ion etching is carried out by gas mixture containing HBr and oxygen.

In FIG. 2g, the photoresist layer 207 and the mask layer 206a are removed. The semiconductor substrate 201b between the deep trenches 201a is a pillar.

In FIG. 2h, the pad layer is removed. The pillared semiconductor substrate 201b between the deep trenches 201a is the active area of forming a MOS.

The deep trench self-alignment process for an active area of a partial vertical cell of the present invention provides an ARC layer on the deep trench capacitor acting as a self-alignment mask. The ARC layer protects the collar insulating layer from etching gas such as gas mixture containing HBr.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications

and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.